

B3 5. (Twice Amended) The ESD protection structure of Claim 8, wherein said third semiconductor region includes an n-well region formed in a p-type semiconductor substrate.

B4 6. (Amended) The ESD protection structure of Claim 5, wherein said second and said fourth semiconductor regions each include a p-base region formed in said n-well region.

7. (Amended) The ESD protection structure of Claim 6, wherein said first and said fifth semiconductor regions each include an n⁺ region formed in one of said p-base regions.

8. (Amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type in contact with said first semiconductor region;

an electrically floating third semiconductor region of said first conductivity type in contact with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type in contact with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type in contact with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region; wherein a first terminal, A, of said ESD structure is connected to said first semiconductor region and said second semiconductor region and a second terminal, K, of said ESD structure is connected to said fourth semiconductor region and said fifth semiconductor region;

a first current source connected to terminal A and a first end of a first resistor whose second end is connected to terminal K; and

a second current source connected to terminal K and a first end of a second resistor whose second end is connected to terminal A.

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9. (Cancelled)

B5
10. (Amended) The ESD protection structure of Claim 8, wherein said first and said second current sources each include a pair of back-to-back Zener diodes.

SM
C5
21. (New) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type in contact with said first semiconductor region;

an electrically floating third semiconductor region of said first conductivity type in contact with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type in contact with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type in contact with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region; wherein a first terminal, A, of said ESD structure is connected to said first semiconductor region and said second semiconductor region and a second terminal, K, of said ESD structure is connected to said fourth semiconductor region and said fifth semiconductor region;

a first pair of back-to-back diodes one of which is connected to terminal A;

a first resistor connected to the other of the first pair of back to back diodes and to terminal K;

a second pair of back-to-back diodes one of which is connected to terminal K; and

a second resistor connected to the other of the second pair of back to back diodes and to terminal K.

22. (New) The ESD protection structure of Claim 21, wherein said first and second pair of back-to-back diodes are back-to-back Zener diodes.

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23. (New) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit comprising:

a two terminal dual-direction semiconductor device, having a first terminal and a second terminal;

a first current source connected to said first terminal and a first end of a first resistor whose second end is connected to said second terminal; and

a second current source connected to said second terminal and a first end of a second resistor whose second end is connected to said first terminal.

24. (New) The ESD protection structure of Claim 23 wherein said first and second current source each include back-to-back Zener diodes.

25. (New) The ESD protection structure of Claim 23 wherein said two terminal dual-direction semiconductor device includes:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type in contact with said first semiconductor region;

an electrically floating third semiconductor region of said first conductivity type in contact with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type in contact with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region; and

a fifth semiconductor region of said first conductivity type in contact with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region; wherein the first terminal is connected to said first semiconductor region and said second semiconductor region and said second terminal of said ESD structure is connected to said fourth semiconductor region and said fifth semiconductor region.

26. (New) The ESD protection structure of Claim 25 wherein said first conductivity type is an n-type semiconductor and said second conductivity type is a p-type semiconductor.

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27. (New) The ESD protection structure of Claim 25 wherein said first conductivity type is a p-type semiconductor and said second conductivity type is an n-type semiconductor.

CH

28. (New) The ESD protection structure of Claim 27 wherein said third semiconductor region includes an n-well region formed in a p-type semiconductor substrate.

BL

29. (New) The ESD protection structure of Claim 28 wherein said second and said fourth semiconductor regions each include a p-base region formed in said n-well region.

30. (New) The ESD protection structure of Claim 29 wherein said first and said fifth semiconductor regions each include an n⁺ region formed in one of said p-base regions.

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